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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/811,401	03/20/2001	Yoshihide Yamaguchi	500.39919X00	4083

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EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/811,401	YAMAGUCHI ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/14/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 17-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-14,20-25,27 and 28* is/are rejected.

7)☒ Claim(s) *2,17-19 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/14/2003 has been entered.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The first paragraph of the abstract is objected to because of inclusion of the phrase "The object of the present invention".

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 5 – 8, 11, 12 – 14, 21, 23 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimomoishizaka, US 6,313,532 in view of Takemura, US 6,184,577.

Regarding claims 1, 12 and 23, Shimomoishizaka teaches a semiconductor device comprising:

- semiconductor element 10 having a plurality of circuit electrodes 11 on a circuit surface thereof,
- a first electrically insulating/protective film 12, which covers an electrode-formed face of the semiconductor element 10 and has an opening part at a position corresponding to said electrode (Fig. 3b), and
- a second electrically insulating layer 20 formed on said first electrically insulating film, wherein said second electrically insulating layer relaxes a stress between said semiconductor device and a substrate on which said semiconductor device is to be mounted, and said second electrically insulating layer is comprised of a thermoplastic resin (low elastic modulus) and has an inclination in an edge portion,
- a wiring layer 32 comprised of a plurality of wirings, each wiring being connected to one of the circuit electrodes and disposed so as to make an electrical connection from said circuit electrodes 11, via the edge portion of the stress

relaxation layer and to a desired site on a surface of the stress relaxation layer 20,

- a surface protecting film 50, which covers surface of the wiring layer so as to expose a prescribed portion on each of the plurality of wirings on the surface of the stress relaxation layer 20, and
- an external connection terminal formed by connecting a bump 40 to said prescribed exposed portion of each of the plurality of wirings with reference to Figs. 1, 2 and 3 and associated descriptions under the best mode for carrying out the invention in columns 5, 6 and 7.

Please note that Shimomoishizaka teaches low elastic modulus stress relaxation layer, which is inherently thermoplastic. Thermoplastic resins are inherently elastic and the thermosetting resins are inherently hard and rigid. Takemura teaches the thermoplastic resins with corresponding modus values (see column 5, line 40), which are equivalent to the elastic modulus values cited by Shimomoishizaka in column 7, line 9.

Regarding claims 5 and 8, Shimomoishizaka teaches low elastic modulus stress relaxation layer, which is inherently thermoplastic and has T_g in the ranges of 150°C (see Takemura in column 7, line 30). Takemura also teaches various low elastic modulus thermoplastic polymers in between column 4, line 61 and column 5, line6.

Regarding claim 6, Shimomoishizaka teaches thermoplastic resin with CTA of 200 ppm/°C in column 7, line 11.

Regarding claims 7 and 13, Shimomoishizaka teaches thickness between 35 – 150 μm in column 7, line 23.

Regarding claims 14 and 24, Shimomoishizaka teaches mounting the semiconductor device on a circuit substrate by connecting external terminal of the device to the electrode of the substrate with reference to Fig. 9.

Regarding claims 11 and 21, these are "product by process claims" and are taught by Shimomoishizaka.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown,* 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 3, 4, 10, 22, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimomoishizaka, US 6,313,532 in view of Takemura, US 6,184,577.

Regarding claims 3 and 4, Shimomoishizaka in view of Takemura fails to teach the melting point of the thermoplastic resin in the stress relaxation layer.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Shimomoishizaka and have a melting point of the stress relaxation layer higher than 350°C for the benefit of providing the soldering layers which has a melting temperature above 350°C and which is formed after forming the stress relaxation layer so that the stress relaxation layer is not damaged during processing the device.

Regarding claims 10, 22, 27 and 28, Shimomoishizaka in view of Takemura fails to teach the wiring layer formed on the stress relaxation layer being wider at the edge portion than on the flat portion. Shimomoishizaka teaches various modifications to the edge with reference to Figs 8 (a) – 8(d).

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Shimomoishizaka and form the wiring to be thicker/wider at the edge of the stress relaxation layer for the benefit of providing a relatively stronger metal layer at the highly stressed position of the edge especially when the edges are deformed as shown in these figures and especially when the deposited layers tend to be thinner on the edges.

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimomoishizaka, US 6,313,532 in view of Takemura, US 6,184,577 as applied to claim 1 above, and further in view of Blalock, US 6,674,158.

Shimomoishizaka in view of Takemura fails to teach the protecting/passivating film constituting of an inorganic and an organic film.

Blalock teaches that passivation film constituting both an inorganic and an organic film for the benefit of providing a barrier to physical damage for semiconductor packaging in column 1, lines 15 – 27.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Shimomoishizaka and provide a passivation film constituting both an inorganic and an organic film for the benefit of providing a barrier to

physical damage for semiconductor packaging as taught by Blalock in column 1, lines 15 – 27.

10. Claims 20 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimomoishizaka, US 6,313,532 in view of Takemura, US 6,184,577 as applied to claim 1 above, and further in view of Ogashiwa, US 5,550,407.

Shimomoishizaka in view of Takemura fails to teach external terminal containing no lead.

Ogashiwa teaches formation of lead-free solder in order to make electrical connection in a semiconductor package (see Tables 25 and 26) and is well known in the art.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Shimomoishizaka and provide a lead-free solder in order to make electrical connection in a semiconductor package. The motivation for doing so would be to use a solder with good electromechanical properties, which is also lead-free, thus making the device more environmentally friendly.

Allowable Subject Matter

11. Claims 2, 17 – 19 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

12. Applicant's argument is about the thermoplastic nature of the stress relaxation layer. As described earlier in rejecting claims 1, 12 and 23, Shimomoishizaka teaches

low elastic modulus stress relaxation layer and is inherently contains thermoplastic material otherwise the layer will be rigid and useless in terms of absorbing any stress.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar

Asok K. Sarkar
February 26, 2004